Fujitsu 90nm Technology Introduction

Fujitsu Limited.

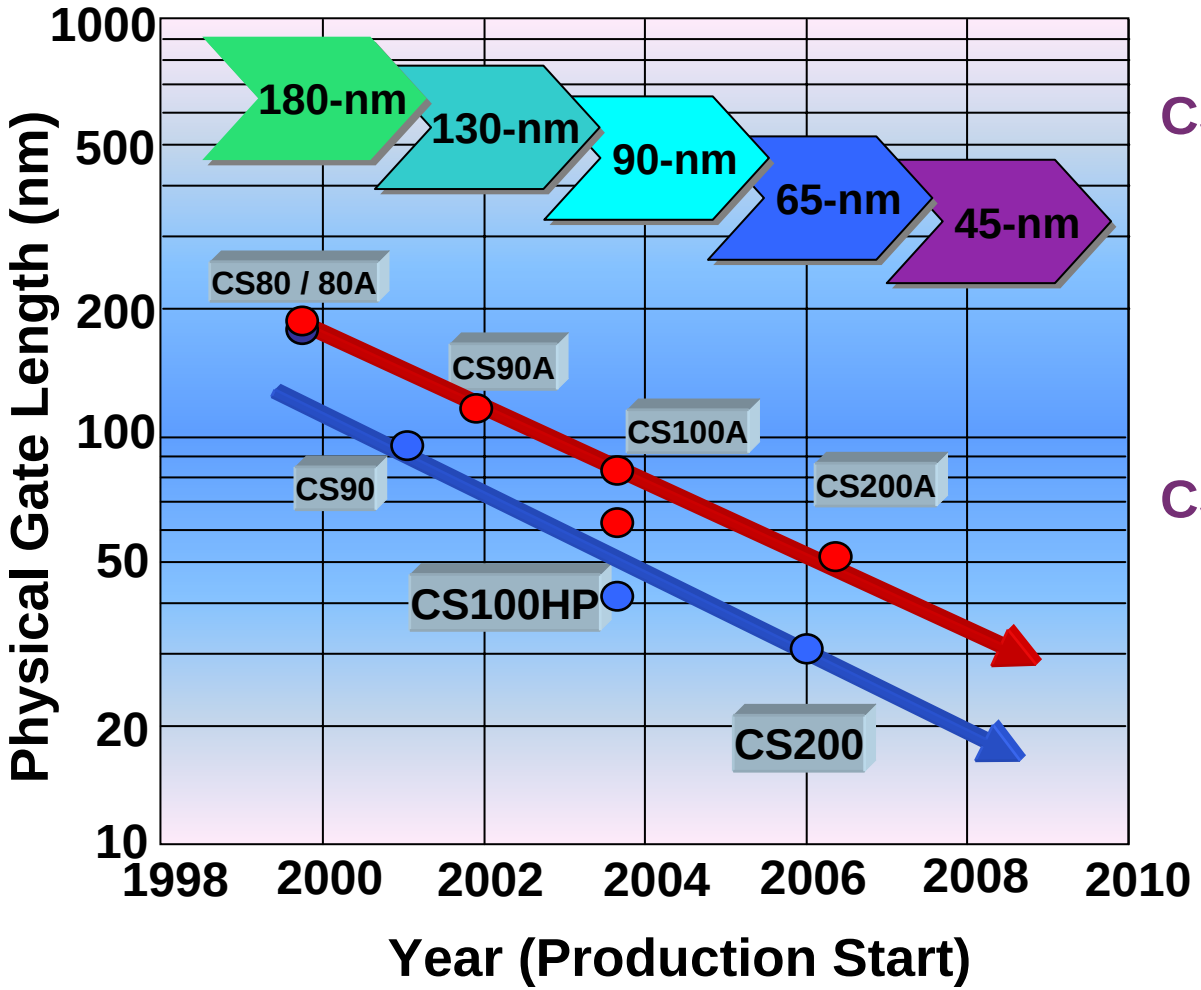
2005.08

Fujitsu Advanced Technology

Leading-edge Technology
Fujitsu 90nm

Fujitsu CMOS Technology Roadmap

FUJITSU



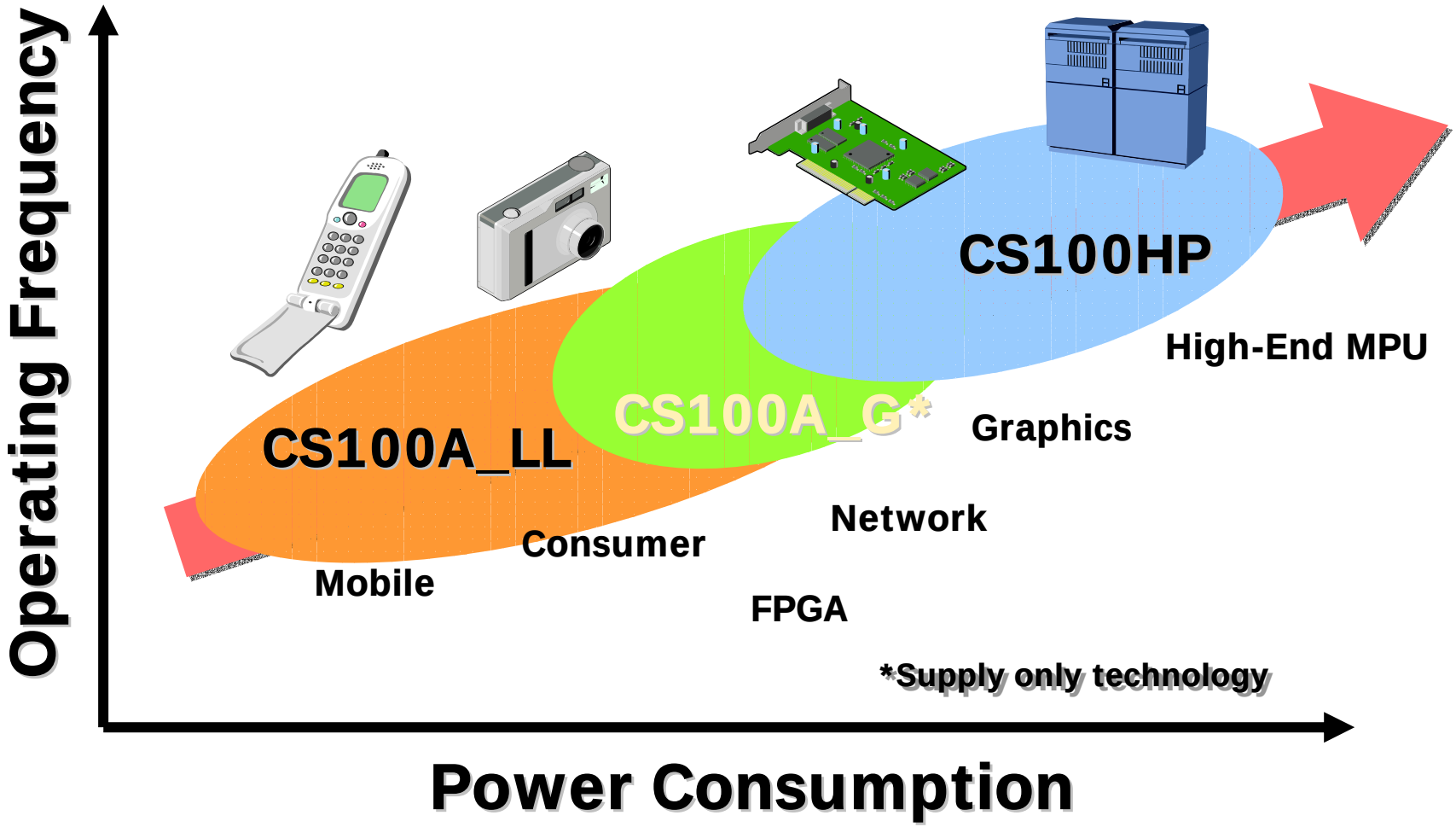
CS100/CS100A (90nm)

- L actual=40-80nm
- SiOC(k:2.9) low-k
- Dual Damascene Cu

CS200/CS200A (65nm)

- L actual=30-50nm
- NCS (Nano-Clustering Silica)

90nm Technology Lineup



Leading-edge Technology
Fujitsu 90nm

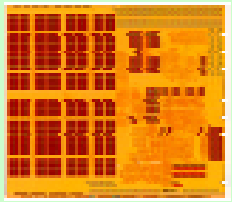
Proven track records of 90nm complex design and products (1)

FUJITSU

- In House Application -

Processors for PRIMEPOWER

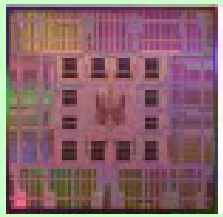
Achieves world-leading performance and reliability

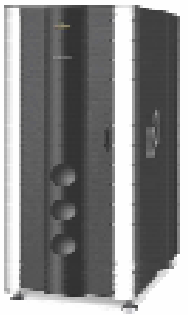


Chipset for PRIMEQUEST

Achieves mainframe-class reliability and scalability

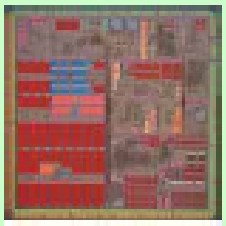
Helped reduce development time





Baseband chip for FOMA 3G mobile phones

LSI power consumption reduced 50%
(compared to existing tech)



Leading-edge Technology
Fujitsu 90nm

Proven track records of 90nm complex design and products (2)

- COT Customers -

FUJITSU

High performance products

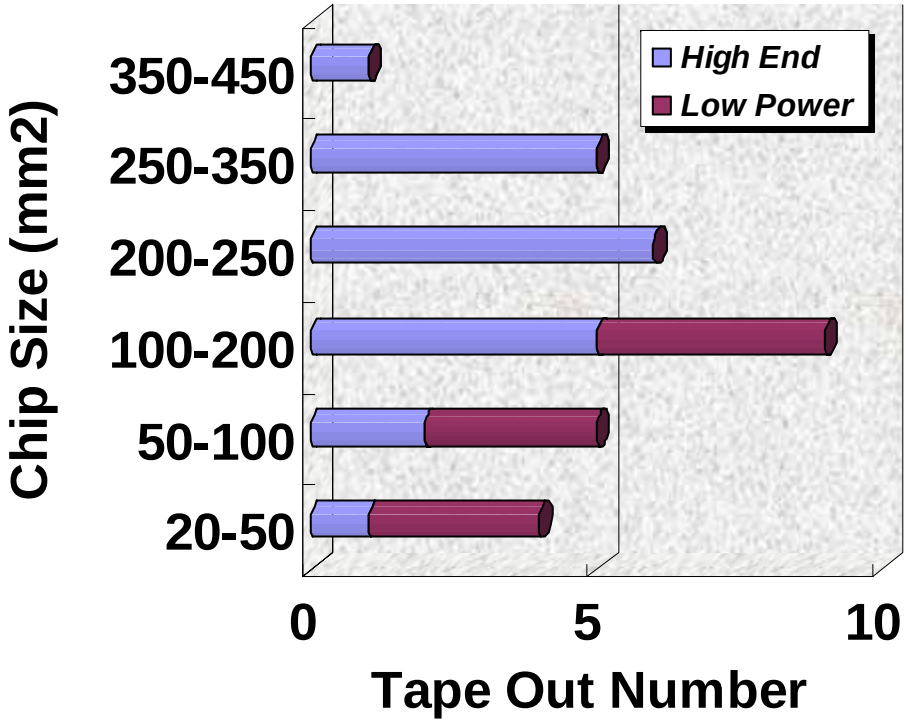
- **PC CPU (Transmeta)**
- **Large scale FPGA (Lattice)**

etc

Low power products

- **Multimedia Processor**
- **Digital AV product**

etc



30 Product Taped Out

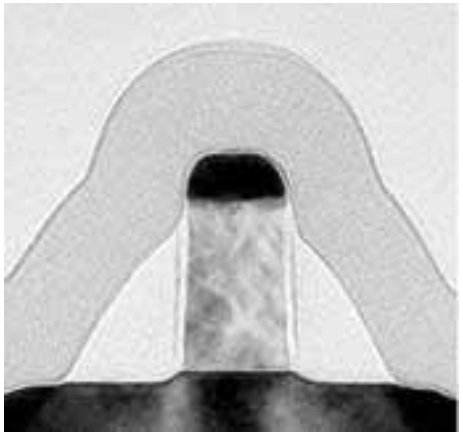
200 prototype wafers delivered

Fujitsu 90nm - Key Features

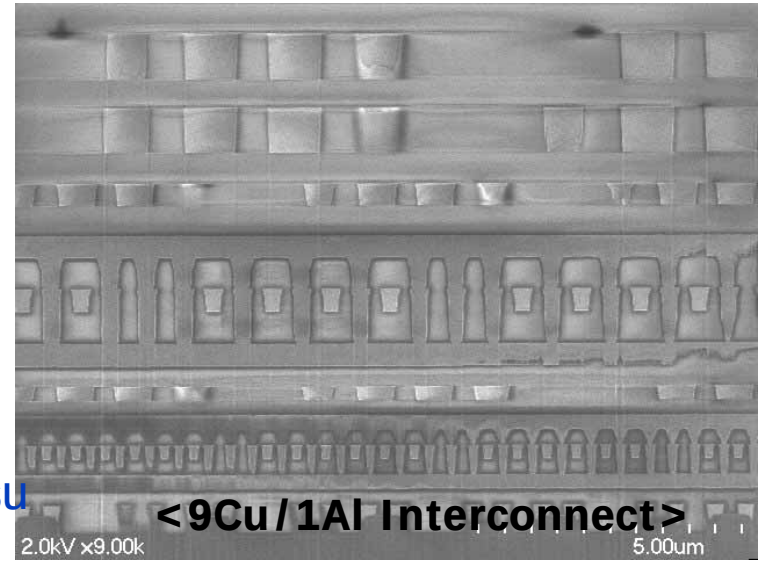
FUJITSU

- **High Performance Transistors**
  - Advanced Lithography and Etch technology to achieve 40nm Gate Length
  - Low Temperature Process for Shallow Junction
  - Process Optimization for High Carrier Mobility
- **High density 6T SRAM**
  - sub-1um^2 cell is available
- ***Dual Damascene Cu + Full Low-k**
- ***Assy and packaging technology**
  - Full Low-K + Pb free bump

    + Large pin count + Large die size**



<40nm Gate>



<9Cu/1Al Interconnect>

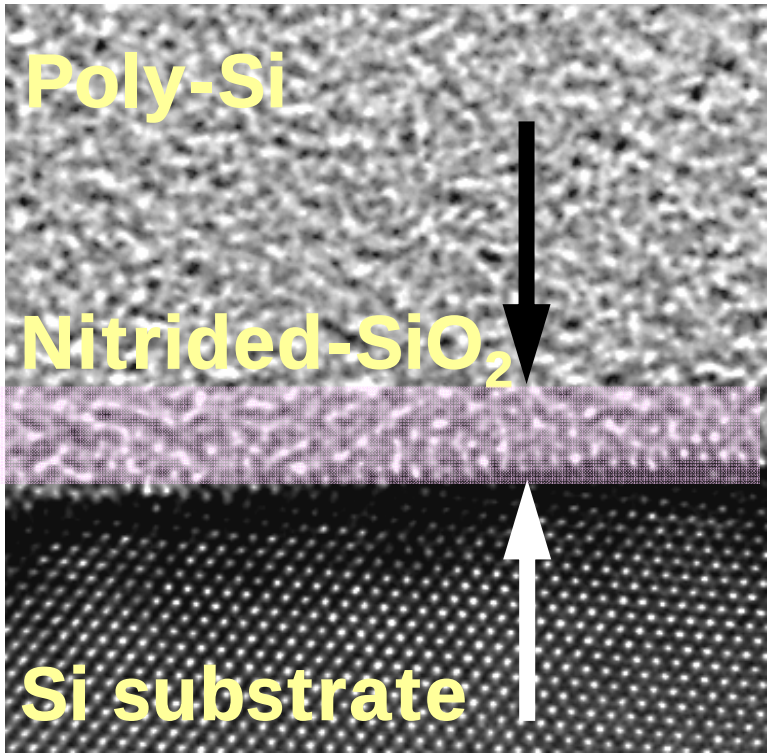
* High performance and high reliability.

** This combination can realize by only Fujitsu in the world.

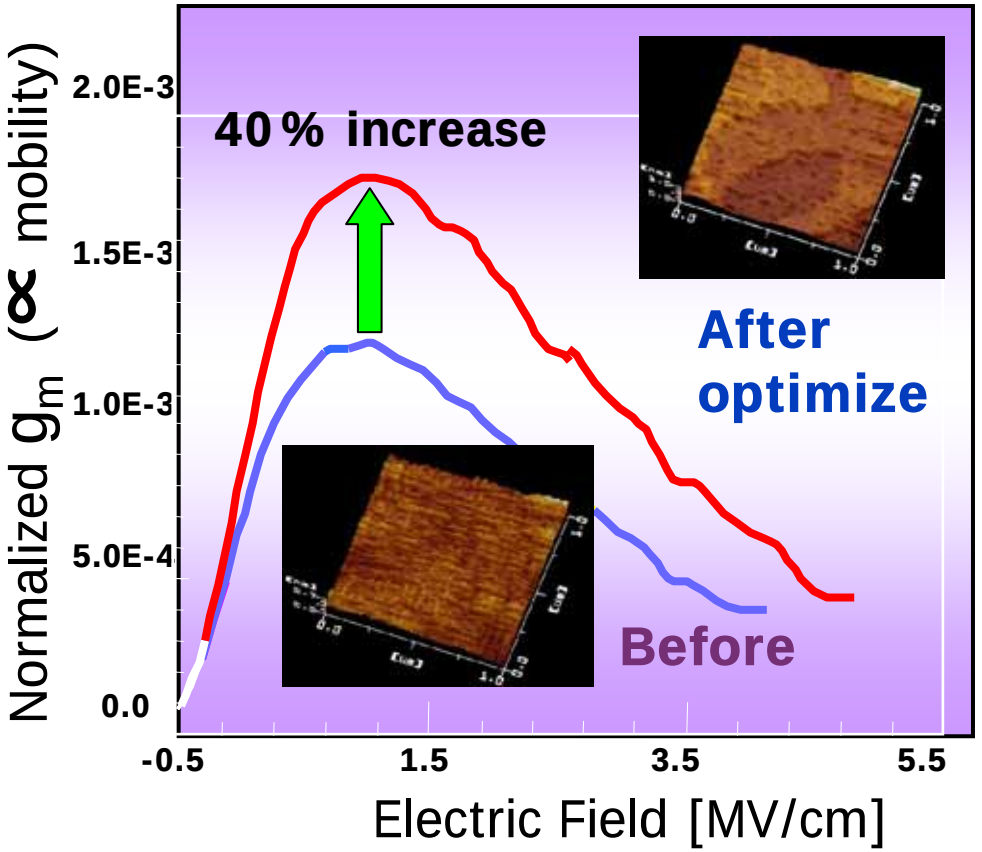
Ultra-Thin Gate Insulator / Mobility Improvement

FUJITSU

1nm-thick Gate Oxide



Surface Cleaning



Advantage of Fujitsu 90nm technology

FUJITSU

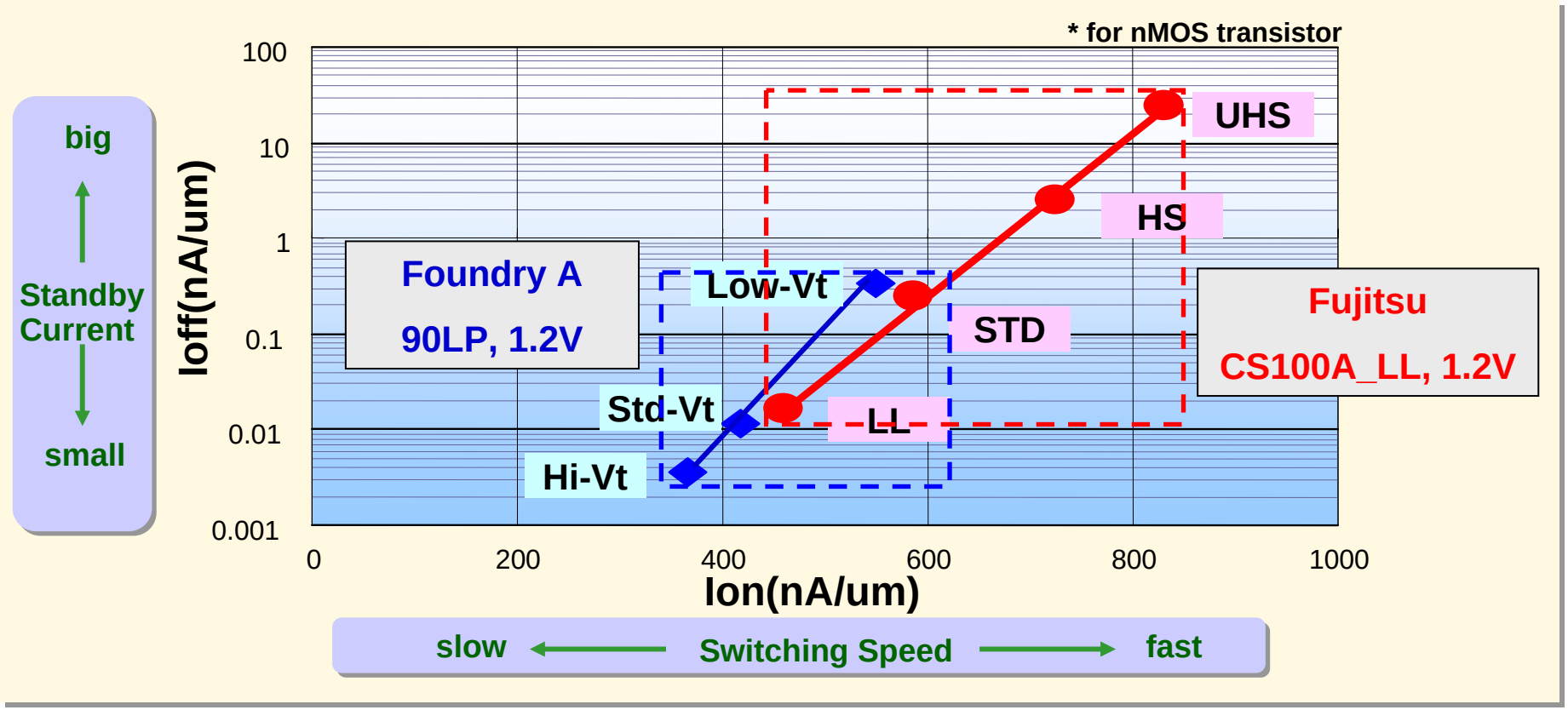
Fujitsu is the World's No.1 Leading Edge Process Technology Supplier

- One customer's benchmark results show Fujitsu's technology has higher performance and low power consumption compared with one of the standard foundry technologies

Speed and Power Comparison	Foundry A	Fujitsu
Speed	100	**125**
Active Power	100	**75**
Stand-by Power	100	**21**

90nm LL Transistor Benchmark

FUJITSU

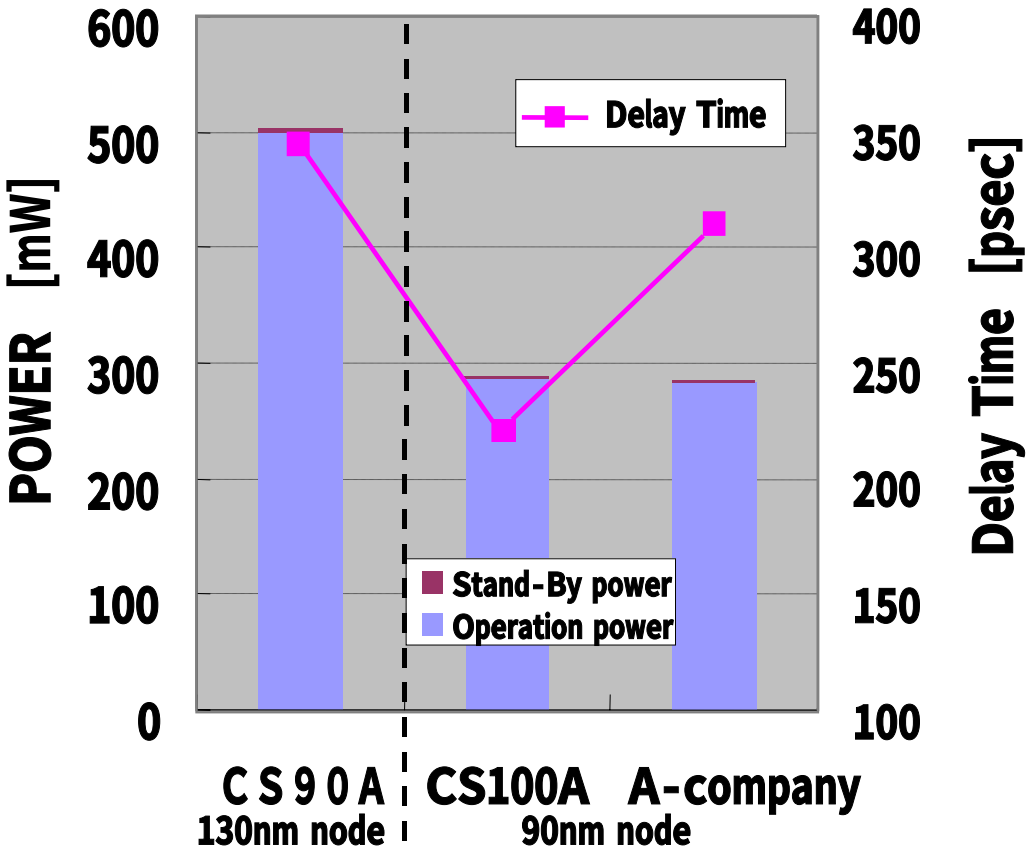


CS100A_LL process covers a *broad range* of requirement for both high performance and low leakage current.

Leading-edge Technology
Fujitsu 90nm

Power/Delay estimation result
Assumption Logic : 1.7Mgate, SRAM : 8Mbit

FUJITSU



Assumption

- Logic : 1.7Mgate, SRAM : 8Mbit
- Power: Tj =85°C, VDD=1.3V, Process Typical
- Delay time: Tj=25°C, VDD=1.2V, Process Typical

■Active power is dominant for total power consumption. Roughly half of 130nm node with 90nm node.

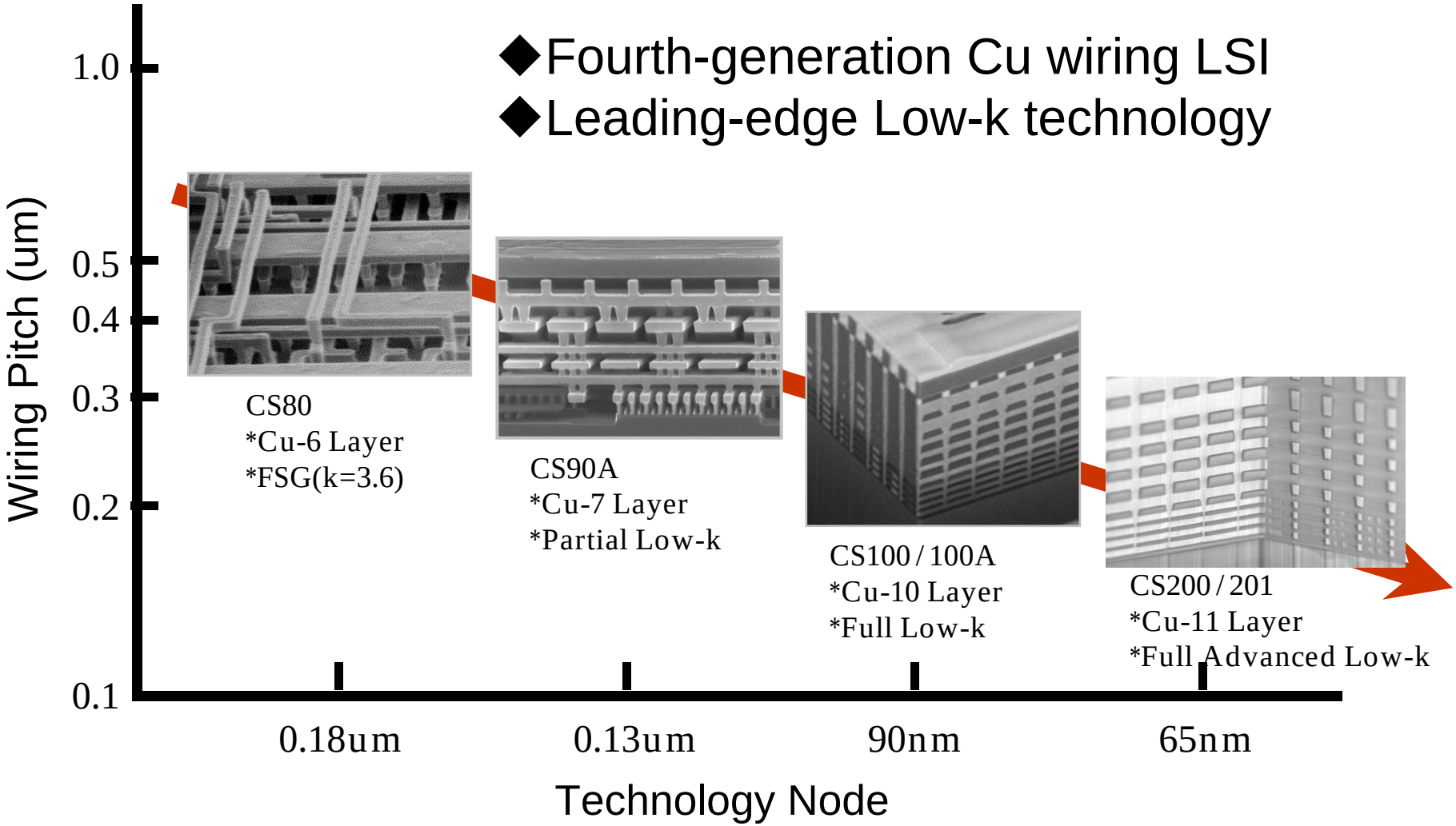
■Total power benefit by evolution.

■Excess Low Leak targeting costs delay time penalty.

Cu/Low-k Integration Technology

FUJITSU

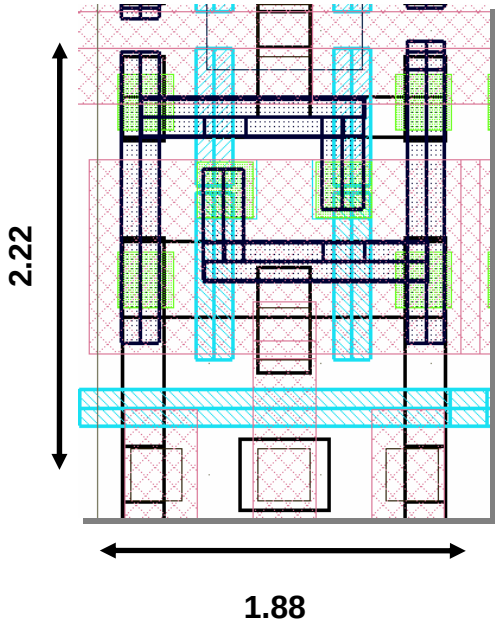
◆Fourth-generation Cu wiring LSI
◆Leading-edge Low-k technology



6T SRAM Cell

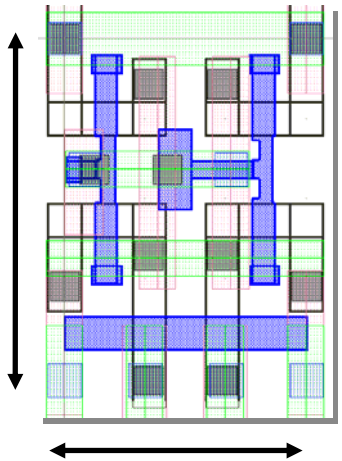
FUJITSU

<CS80A /180nm>



4.18um²

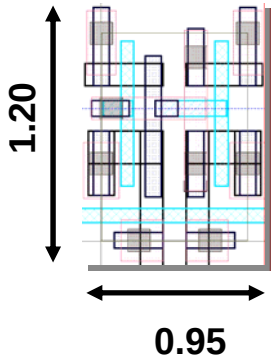
<CS90A/130nm>



1.98um²

<CS100A/90nm>

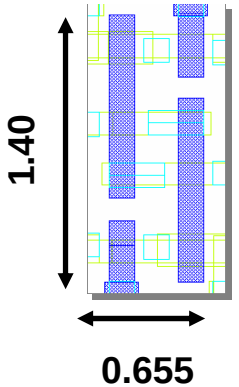
Conventional Type: Verified



1.14um²

16 - 512Kbit

Symmetrical Type: For Bigger size



0.917um²

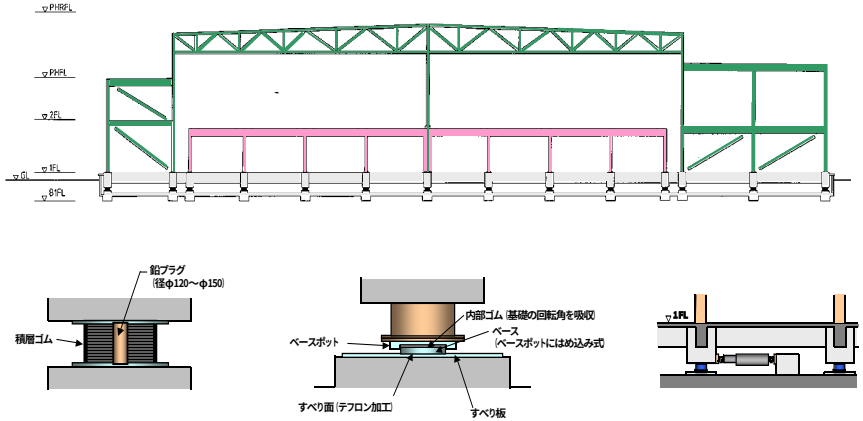
32K - 8Mbit

90/65nm 300mm New Fab.

FUJITSU

Outlook of new fab.

World first semiconductor fab. with a micro vibration control & seismically isolated structure

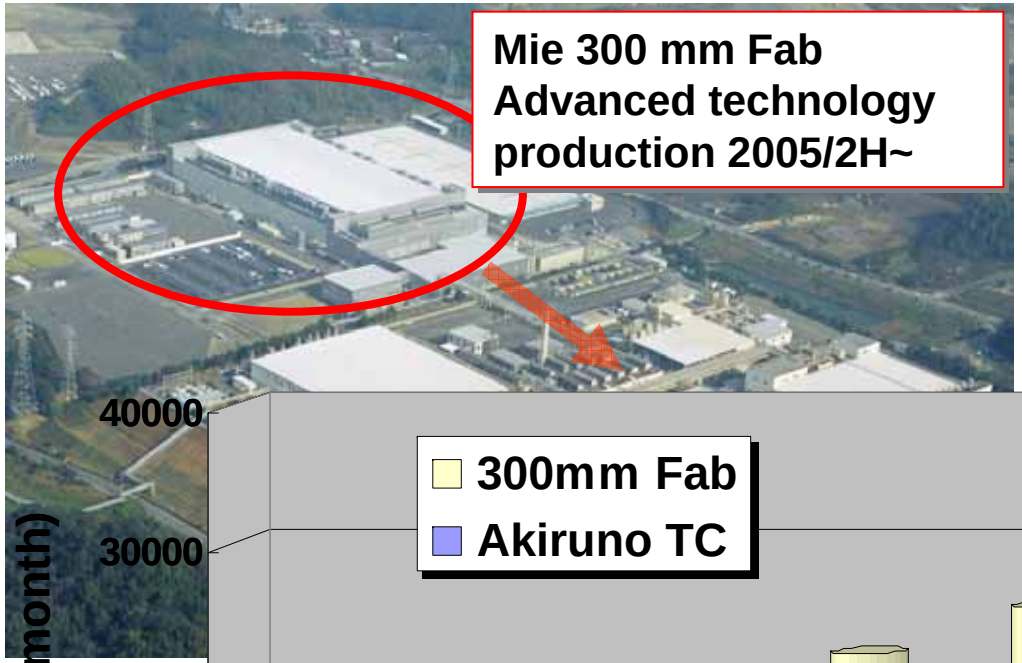


Mie New Fab. Milestone

- Apr. 21, 2004
  Ceremony for sanctifying ground
- Nov. 20, 2004
  Completion of construction
- Apr. 1, 2005
  Formal operation starts
- Sept. 9, 2005
  Volume shipment

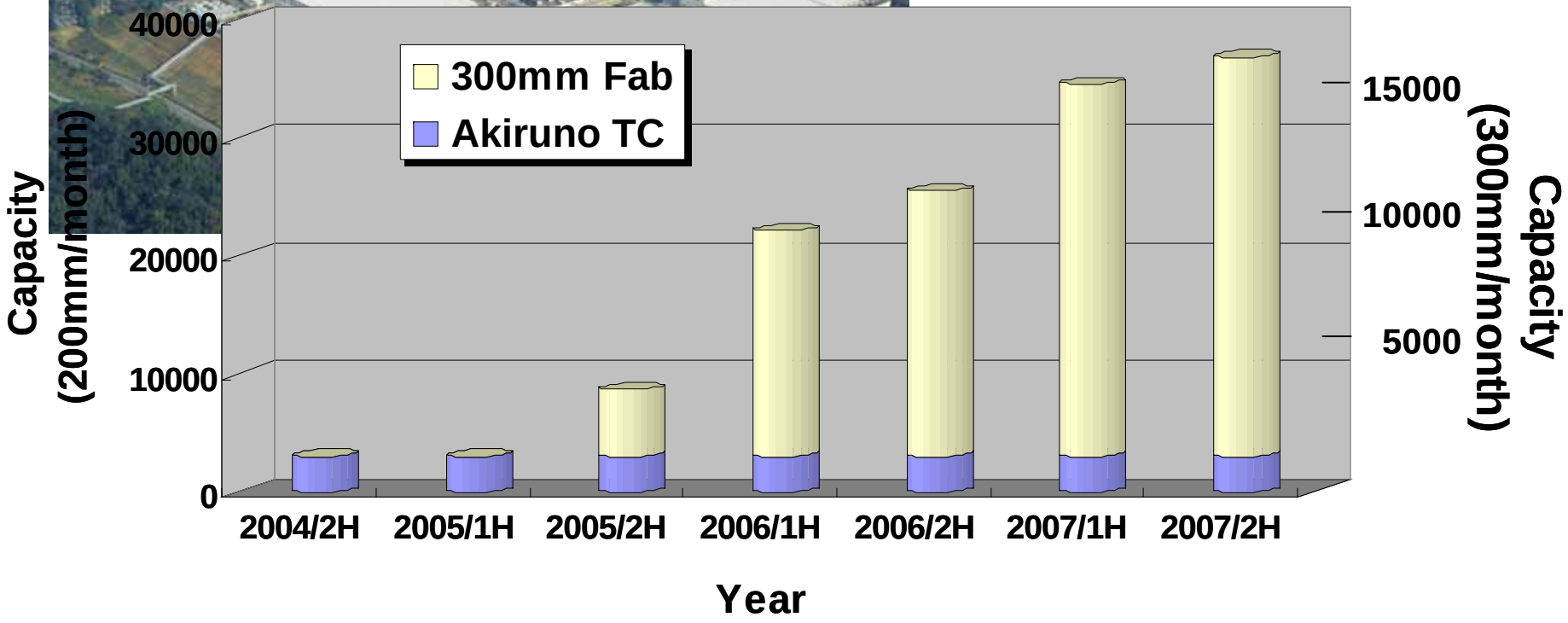
300mm foundry capacity for 90nm/65nm

FUJITSU



Mie 300 mm Fab
Advanced technology
production 2005/2H~

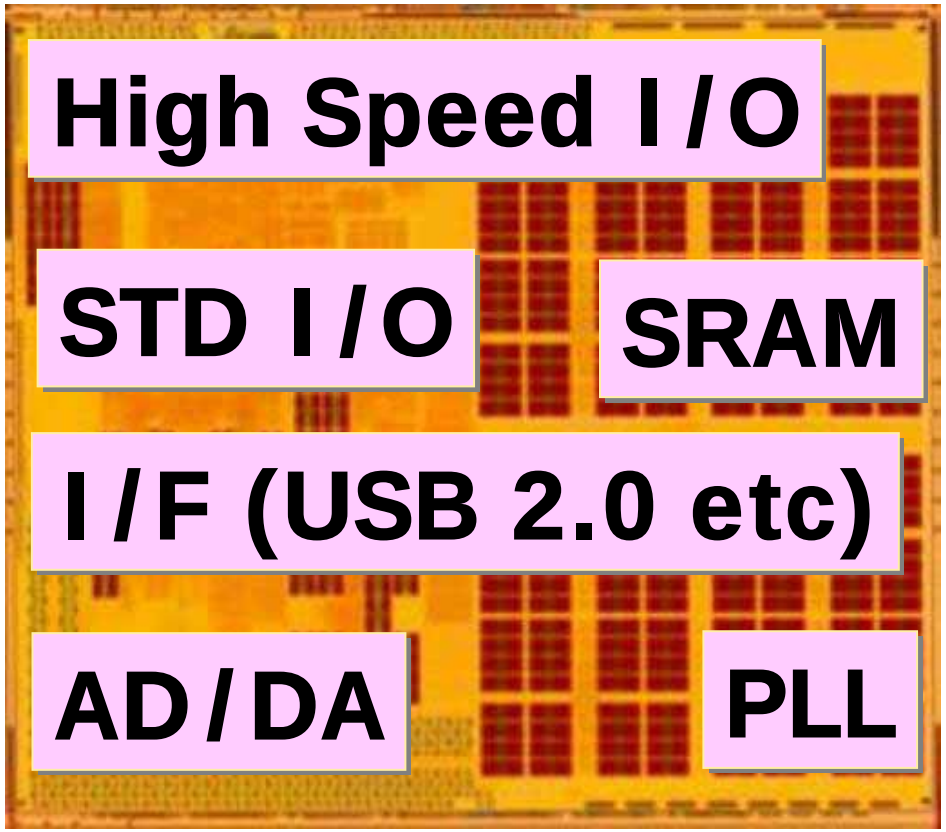
Akiruno TC 200mm
Advanced technology
development and
production



Extensive IP line up

FUJITSU

- Customers are satisfied with the Si verified IP.
- Fujitsu provide extensive IP line up.



*** Chip photo is not related on each IP.**

Fujitsu Foundry Services

Fujitsu launched pure foundry business

Fujitsu announced " Fujitsu launched pure foundry business as primary to keep pace with market shift from ASIC to foundry .

This advertisement is published in "Nikkei electronics 2004 12-6, page 100-101" , which is one of the major magazine of electronics in Japan.

In 2005 April, Fujitsu has released the similar advertisement in U.S.A.

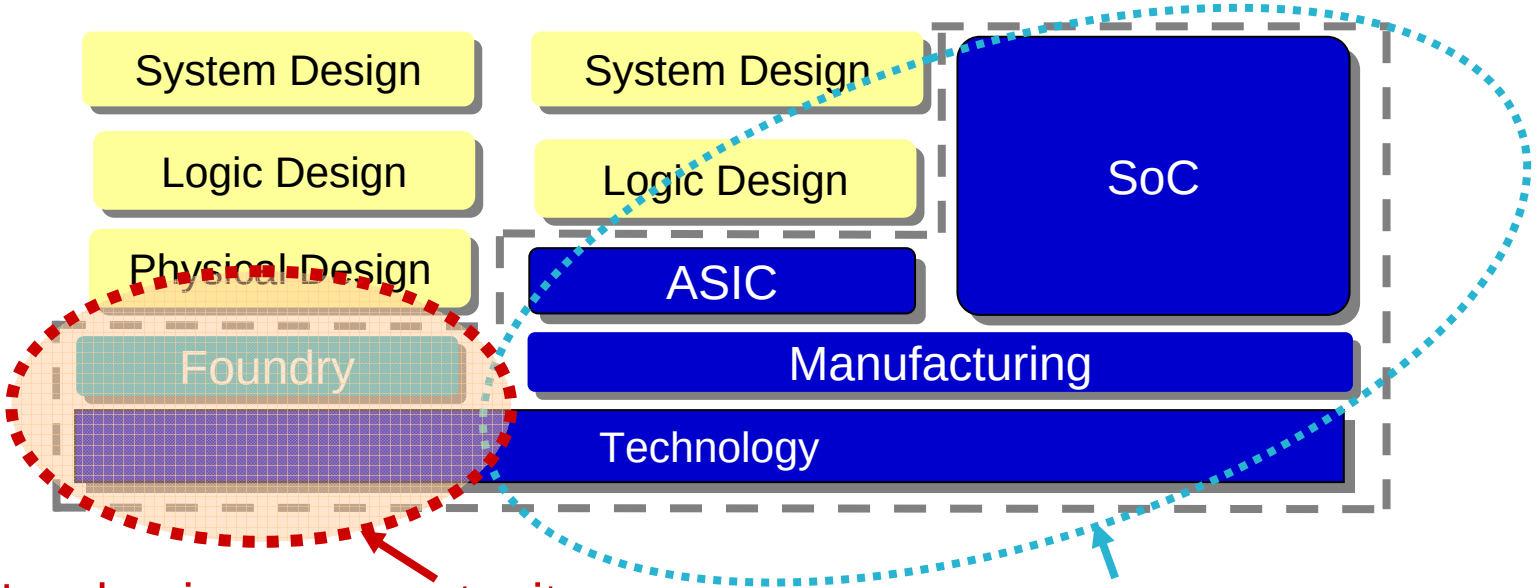
Changing Business Environment

FUJITSU

◆Customers' needs are changing with evolution in LSI development

➡ Customers require integrated design and engineering and flexible manufacturing capabilities

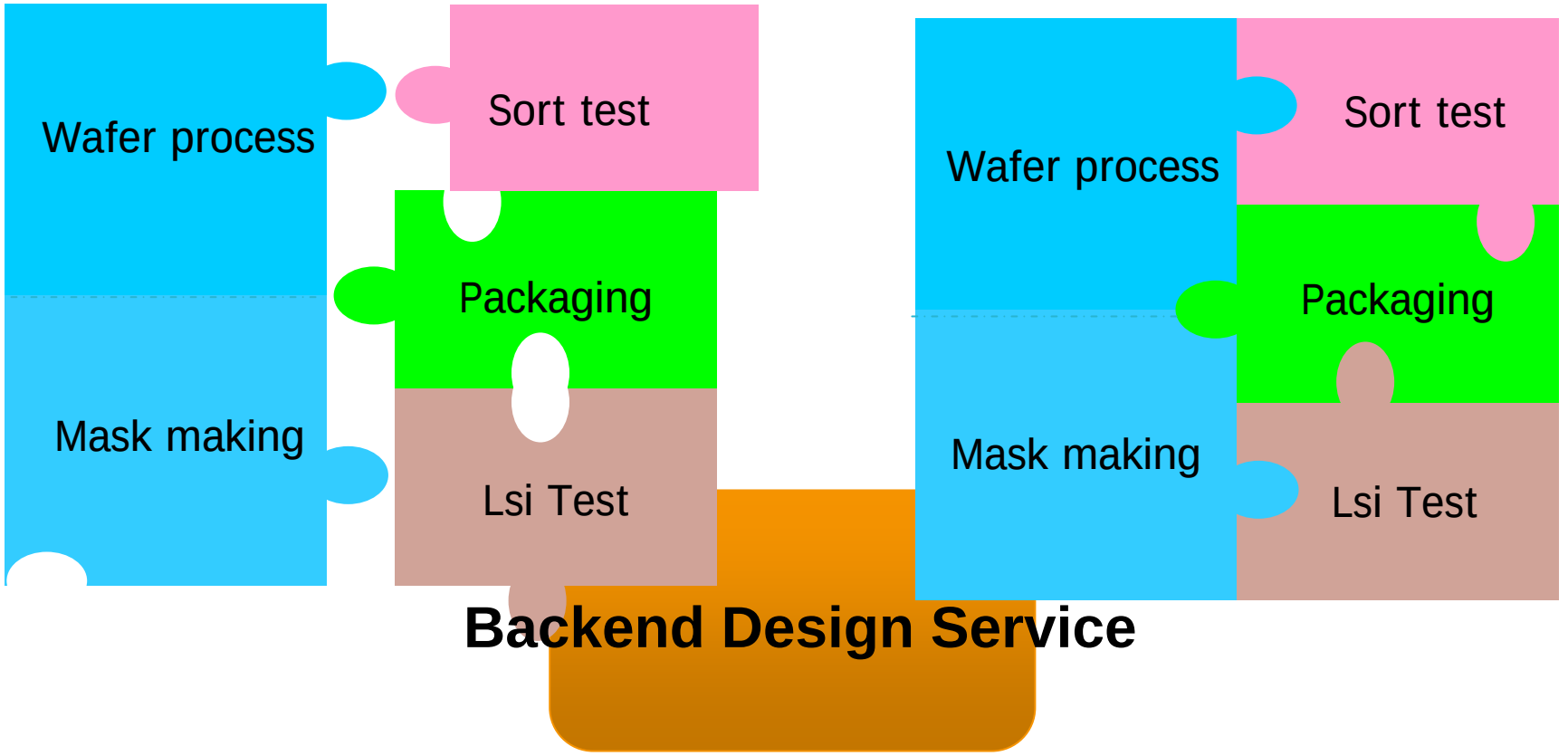
Strong Appeal as New IDM Vendor



Full Turnkey Foundry Service option

FUJITSU

Customer can select service and biz model.



EDG in Japan

FUJITSU

Iwate Plant
[Memory, Microcomputer, Logic]

FIM (Miyagi) Assembling

FIM (Aizu) Assembling & Test

Akiruno TC (Tokyo)
R&D (90nm～)

Aizu Wakamatsu Plant

FIM (Gifu) Assembling & Test

*:300mm FAB 90nm/65nm

FIM (Kagoshima)
Assembling & Test

Mie Plant

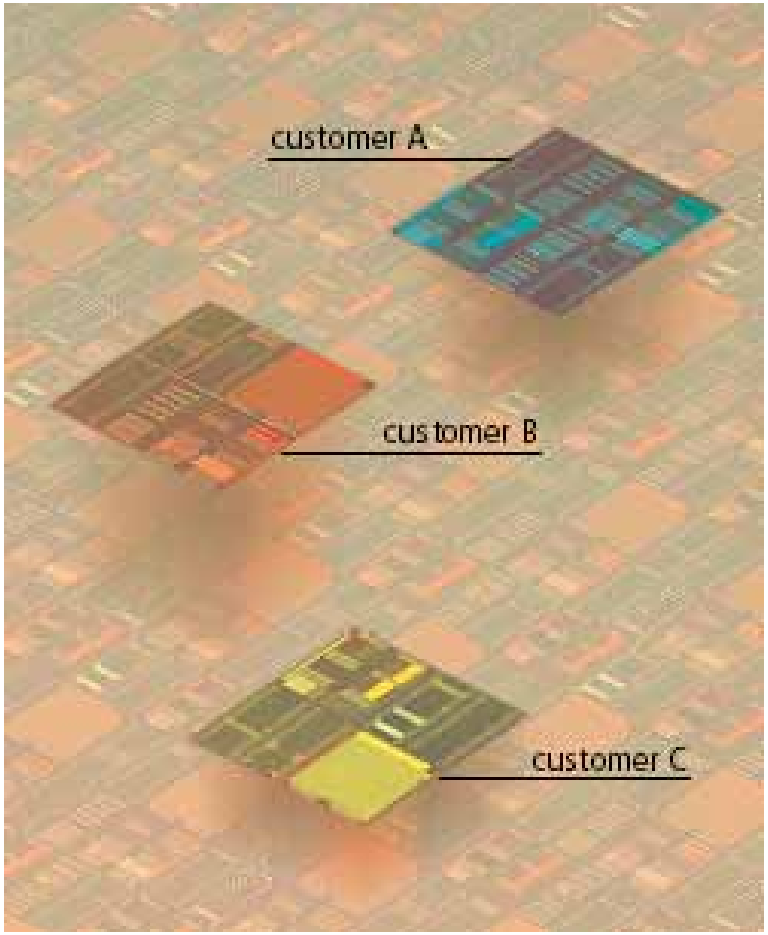
FIM : Fujitsu
Integrated
Microtechnology

SiExpress™

FUJITSU

SiExpress™ is a pre-production service where customers save cost by sharing mask sets and wafer, called multi-project-wafer.

SiExpress™ service provides completely consistent samples which enable your real product's performance evaluation.

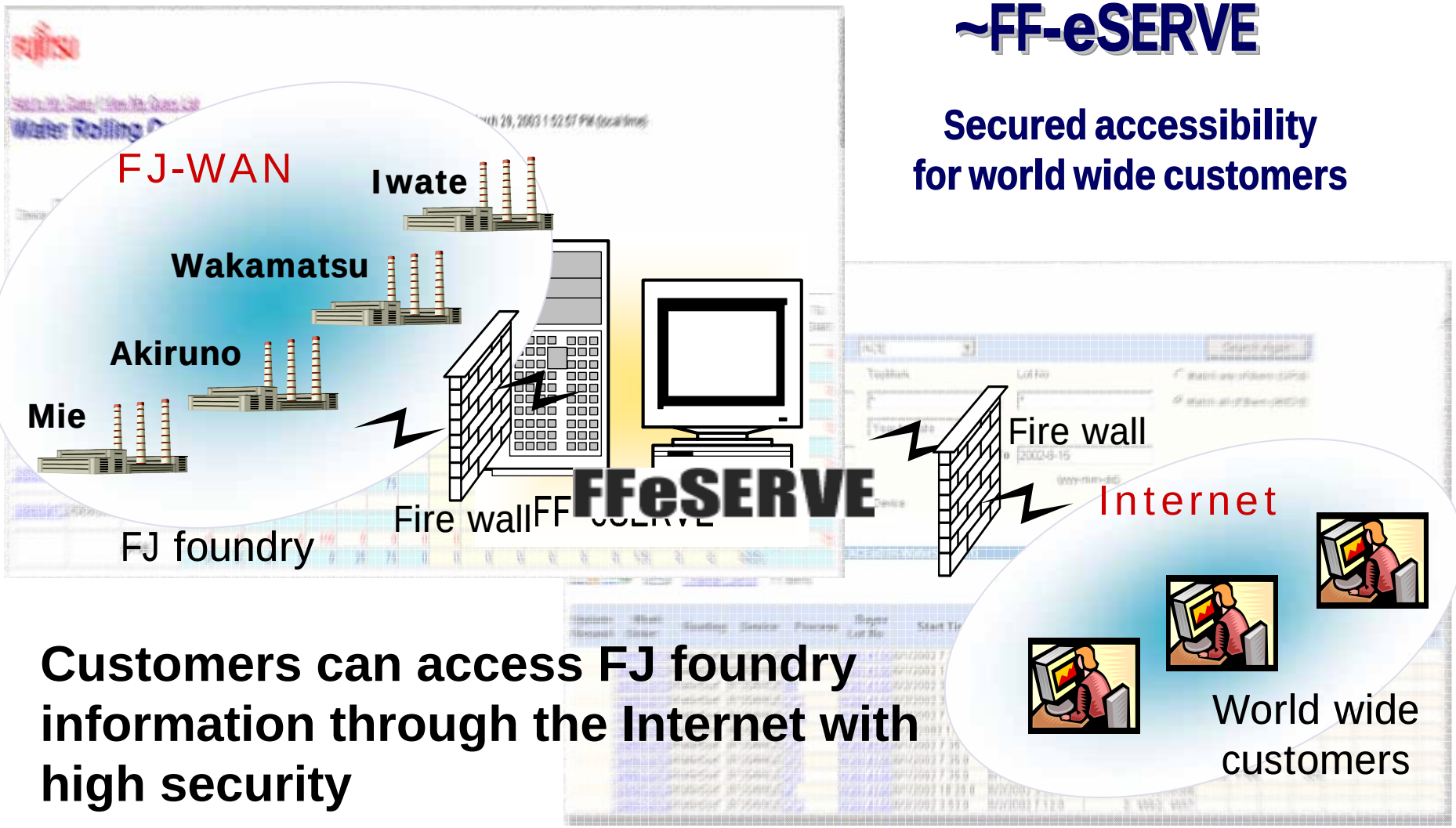


Sample forms

- Bare Chips
- Package chips

Fab information system

FUJITSU



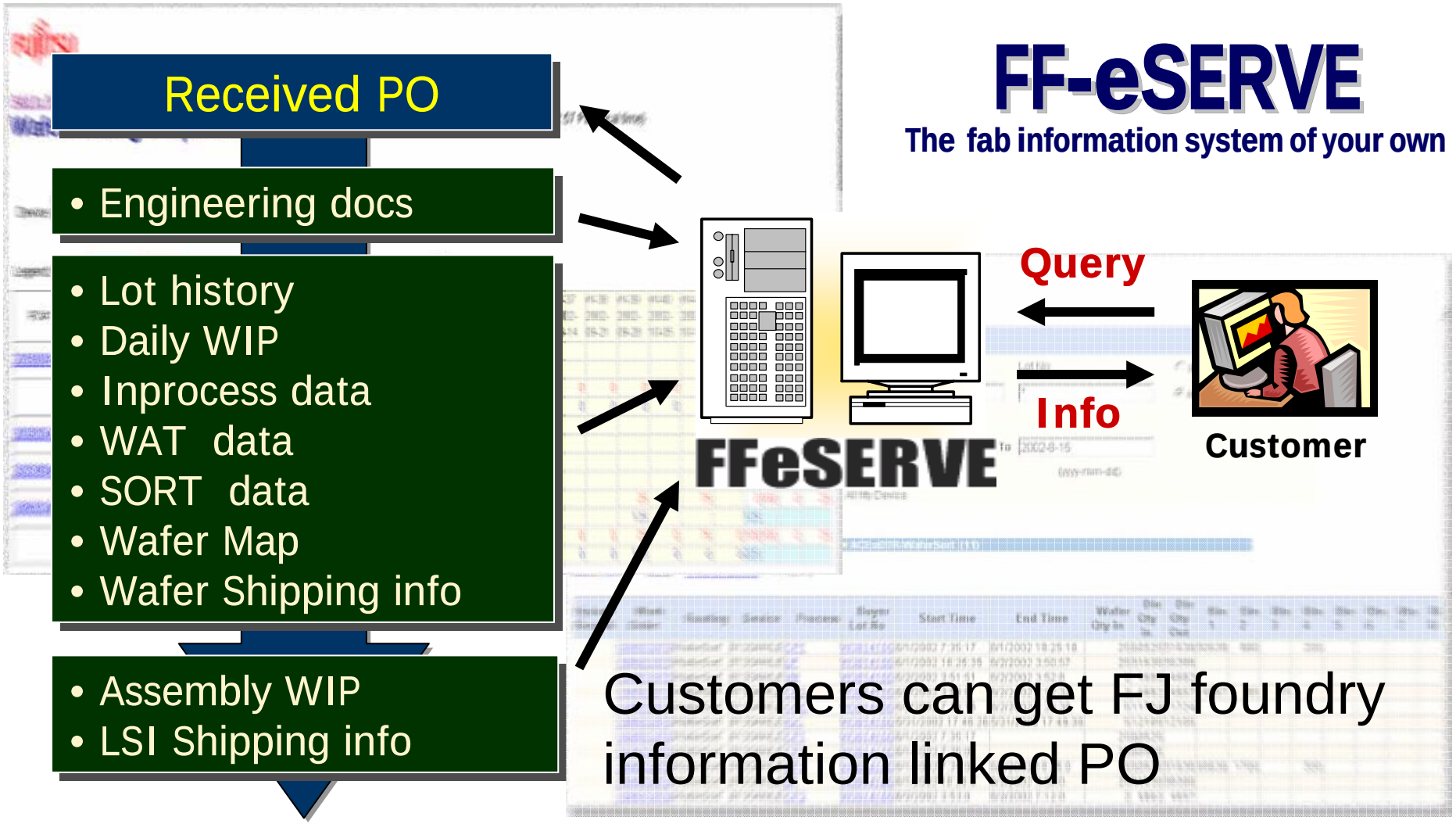
~FF-eSERVE

Secured accessibility for world wide customers

Customers can access FJ foundry information through the Internet with high security

Fab information linked customer's PO

FUJITSU



Why Fujitsu foundry?

- Fujitsu launched foundry biz.
- Provide 300mm capacity for “Foundry Customer”
- Customer can enjoy the Fujitsu’s high performance and low leakage 90nm technology.
- Matured 90nm device production
  - From high end to low power devices
  - Higher yield than other fab.
- Extensive IP line up

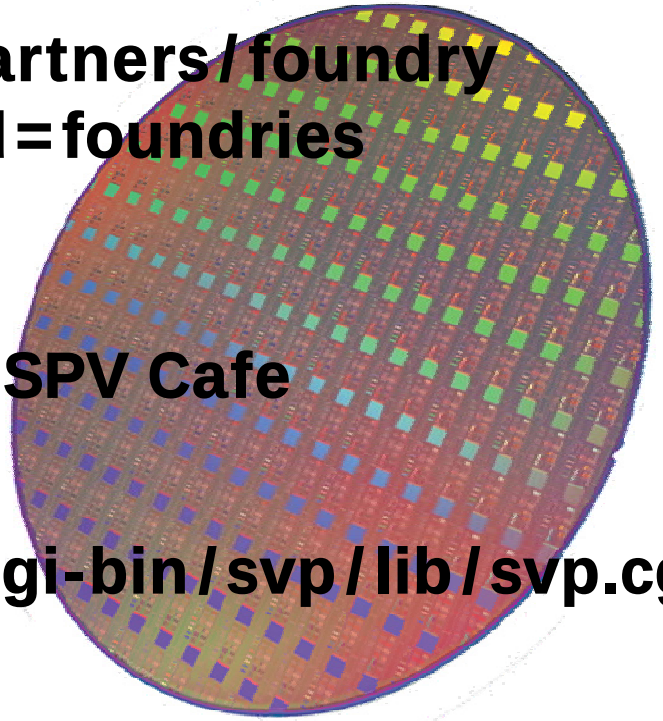
EDA tool vendor's support

FUJITSU

cadence®

Cadence Foundry Program

http://www.cadence.com/partners/foundry_program/index.aspx?lid=foundries



SYNOPSYS®

Synopsys SPV Cafe

http://www.synopsys.com/cgi-bin/svp/lib/svp.cgi

Standard Cell

1. Standard cell

1-1. CS100A_LL

Tr. / Cell Height	LL	STD	HS
9grid	Now	Now	Now
12grid	Now	Now	Now

1-2. CS100HP

Tr. / Cell Height	HiVT	STD	HS
9grid	3Q / 2005	3Q / 2005	NA

LL : Low-Leak Tr. , STD : Standard Tr. , HS : High-Speed Tr. , HiVT : High-Vth Tr.

I / O Cell

2. I/O cell

2-1. CS100A_LL

Interface	Status	Note
3.3V LVCMOS	Now (63cells)	for 3.3V Process
3.3V PCI	Now (5cells , 66/33MHz)	for 3.3V Process
SSTL-2	Now (5cells , 400Mbps)	for 3.3V Process
LVDS	4Q / 2005 (5cells , 333MHz)	for 3.3V Process

2-2. CS100HP

Interface	Status	Note
2.5V LVCMOS	3Q / 2005 (TBD)	for 2.5V Process

Memory

3. SRAM / ROM / Register File

Type	CS100A_LL		CS100HP	
	Tr. Type (Cell / Peripheral)	Status	Tr. Type (Cell / Peripheral)	Status
1RW SRAM	LL / LL	Now	HiVT / HiVT	On demand
	LL / STD	Now	HiVT / STD	On demand
	LL / HS	Now	HiVT / HS	On demand
2RW SRAM	LL / LL	Now	HiVT / HiVT	On demand
	LL / STD	Now	HiVT / STD	Now *1
	LL / HS	Now	HiVT / HS	On demand
ROM	LL / LL	Now	HiVT / HiVT	On demand
	LL / HS	Now	HiVT / STD	On demand
1R1W Reg. File	LL / LL	Now	HiVT / HiVT	On demand
	LL / STD	Now	HiVT / STD	On demand
	LL / HS	Now	HiVT / HS	On demand
2R2W Reg. File	LL / LL	Now	HiVT / HiVT	On demand
	LL / STD	Now	HiVT / STD	On demand
	LL / HS	Now	HiVT / HS	On demand

*1 : Virage's IP

LL : Low-Leak Tr. , STD : Standard Tr. , HS : High-Speed Tr. , HiVT : High-Vth Tr.

I/F Macro, ARM

I/F Macro

	Macro	Functions	Specifications	Design completion	Evaluation completion (SiliconProven)	Note (Procurement or Development)
1	USB2.0 Device	USB2.0(HS) Device PHY	Now	2005/5/E	2005/8/E	Development
2	USB2.0 Host	USB2.0(HS) Host PHY	TBD	TBD	TBD	Development
3	USB2.0 OTG	USB2.0(HS) OTG PHY	Now	2005/7/E	2005/8/E	Procurement
4	IEEE1394.a	IEEE1394.a AV-protocol only (LINK + PHY)	Now	2005/6/E	2005/11/E	Development
5	S-ATA	S-ATA 1.5G Host PHY	2005.6.30(PHY)	2005.10.31(PHY)	2006.3.31(PHY)	Procurement
6		S-ATA 3.0G Host PHY	TBD	TBD	TBD	TBD
7	PCI-Express	PCI-Express 2.5G Endpoint PHY	2005.5.31(PHY)	2005.10.31(PHY)	2006.3.31(PHY)	Development
8	DRAM Controller	DDR2 400～533Mbps x 32	2005/5/E	2005/6/B	2005/9/E	Development
9		DDR2 400～533Mbps x 16	2005/5/E	2005/8/B	2005/11/E	Development
10		DDR2 ～800Mbps x 16	2005/9/B	2006/4/B	2006/8/E	Development
11	UWB	UWB	TBD	TBD	TBD	Joint Development

ARM

	Macro	Functions	Specifications	Design completion	Evaluation completion (SiliconProven)	Note (Procurement or Development)
1	ARM	ARM7TDMI-S	Now	We will deliver the library two months after the business fixation.		
2		ARM926EJ-S	Now			
3		ARM946E-S	Now			
4		ARM1176JZF-S	Now			

PLL, DLL

	Macro	Functions	Specifications	Design completion	Evaluation completion (SiliconProven)	Note (Procurement or Development)
1	PLL	Fout:100-150MHz, Fin:12.5-150MHz, N=1-8, Power:1mW	NOW	NOW	NOW	Development
2		Fout:150-200MHz, Fin:10-200MHz, N=1-15, Power:1mW	NOW	NOW	NOW	Development
3		Fout:200-230MHz, Fin:10-200MHz, N=1-16, Power:1mW	NOW	NOW	NOW	Development
4		Fout:100-300MHz, Fin:8-150MHz, N=2-38, Power:3mW	NOW	NOW	NOW	Development
5		Fout:250-600MHz, Fin:8-200MHz, N=2-66, Power:4mW	NOW	NOW	NOW	Development
6		Fout:400-800MHz, Fin:10-50MHz, N=12-40, Power:6mW	NOW	NOW	NOW	Development
7		Fout:500-900MHz, Fin:6.25-150MHz, N=6-96, Power:6mW	NOW	NOW	NOW	Development
8		Fout:600-1200MHz, Fin:6-80MHz, N=6-80, Power:7mW	NOW	NOW	NOW	Development
9		Fout:20-32MHz, Fin:0.3-50MHz, N=30-66, Power:4mW	2005/6/E	2005/6/E	2005/11/E	Development
10		Fout:50-62MHz, Fin:0.3-50MHz, N=12-66, Power:4mW	2005/6/E	2005/6/E	2005/11/E	Development
11		Fout:90-150MHz, Fin:1.5-50MHz, N=32-66, Power:4mW	2005/6/E	2005/6/E	2005/11/E	Development
12		Fout:1200-1500MHz, Fin:24-100MHz, Power:10mW	2005/12/E	2005/12/E	2006/3/E	Development
13		Fout:1500-1800MHz, Fin:24-200MHz, Power:12mW	2005/12/E	2005/12/E	2006/3/E	Development
14		Fout:24.576MHz, Fin:24KHz, N=1024, Power:10mW (High Multiply)	2005/6/E	2005/7/E	2005/12/E	Development
15		Fout:150-300MHz, Fin:18.75-37.5MHz, N=8, Power:15mW (SSCG) (The available Fout[MHz]/Fin[MHz] pair is only five cases or 150/18.75,192/24,200/25,266/33.25,300/37.5)	2005/8/E	2005/8/E	2005/9/E	Development

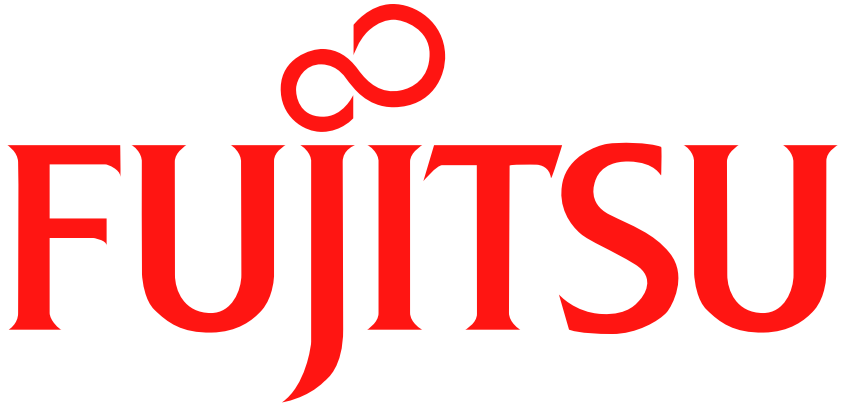
*Analog Capacitor is 3.3V Poly-Diffusion capacitor.

	Macro	Functions	Specifications	Design completion	Evaluation completion (SiliconProven)	Note (Procurement or Development)
1	DLL(Analog)	Number of TAP:16, DQS≦133MHz, Power:10mW	NOW	Now	Now	Development

*Analog Capacitor is 3.3V Poly-Diffusion capacitor.

ADC, DAC

	Macro	Functions	Specifications	Design completion	Evaluation completion (SiliconProven)	Note (Procurement or Development)	Note VDD=3.3V(typ)
1	ADC	10bit 1MS/s	now	now	now	Development	Planning of Improvement Now Designing (with Input sw)
2		10bit 1MS/s	now	now	2005.9.E	Development	With 17ch Input Switch
3		12bit 1MS/s	2005.7.E	2005.8.E	2005.12.E	Development	Single Input
4		6bit 108MS/s	now	now	2005.7.E	Development	Single Input
5		8bit 54MS/s	now	now	2005.7.E	Development	Single Input
6		10bit 30MS/s	now	now	2005.11.E	Development	Single Input
7		10bit 80MS/s	now	now	2005.10.E	Development	FMSL Differential Input
8		10bit 150MS/s	2005.7.E	2005.9.E	2006.1.E	Development	FMSL Differential Input
9	DAC	8bit 300kHz	now	now	now	Development	Voltage Output Low Power
10		8bit 1MHz	now	now	2005.7.E	Development	Voltage Output
11		10bit 300kHz	now	now	2005.7.E	Development	Voltage Output Low Power
12		10bit 1MHz	now	now	2005.7.E	Development	Voltage Output
13		10bit 30MHz	now	now	now	Development	Current Output VDD=2.5V
14		10bit 30MHz	now	now	2005.7.E	Development	Current Output With built-in resistance
15		10bit 54MHz	now	now	2005.11.E	Development	Current Output
16		10bit 110MHz	2005.10.E	2005.10.E	2006.1.E	Development	Current Output



THE POSSIBILITIES ARE INFINITE